

# **Device-Level BTI-induced Timing Jitter Increase in Circuit-Speed Random Logic Operation**

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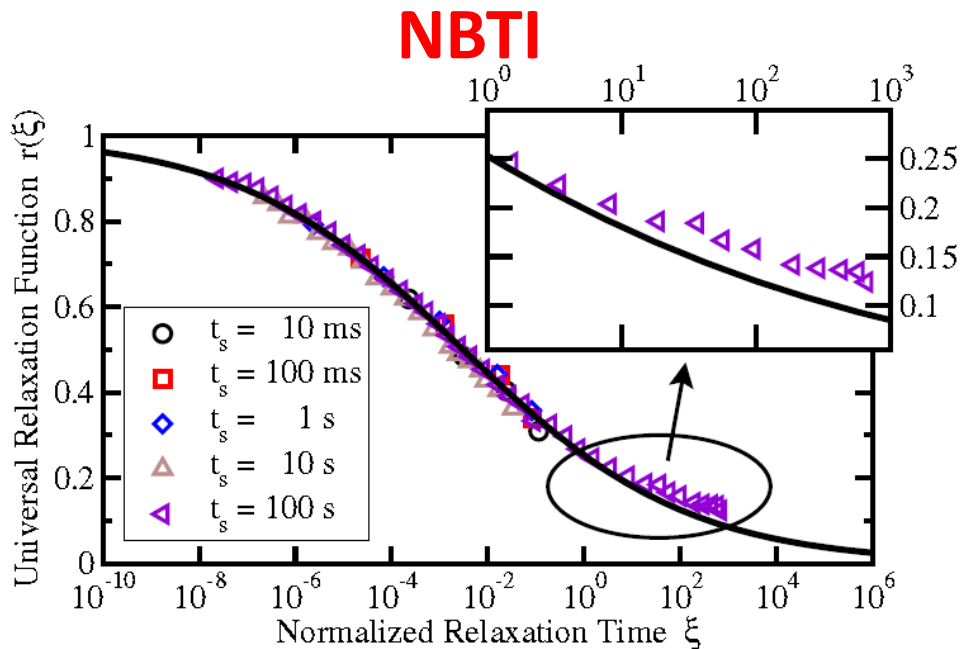
# Hot topics in advanced CMOS:

Bias-Temperature-Instability (BTI) → serious reliability problem.

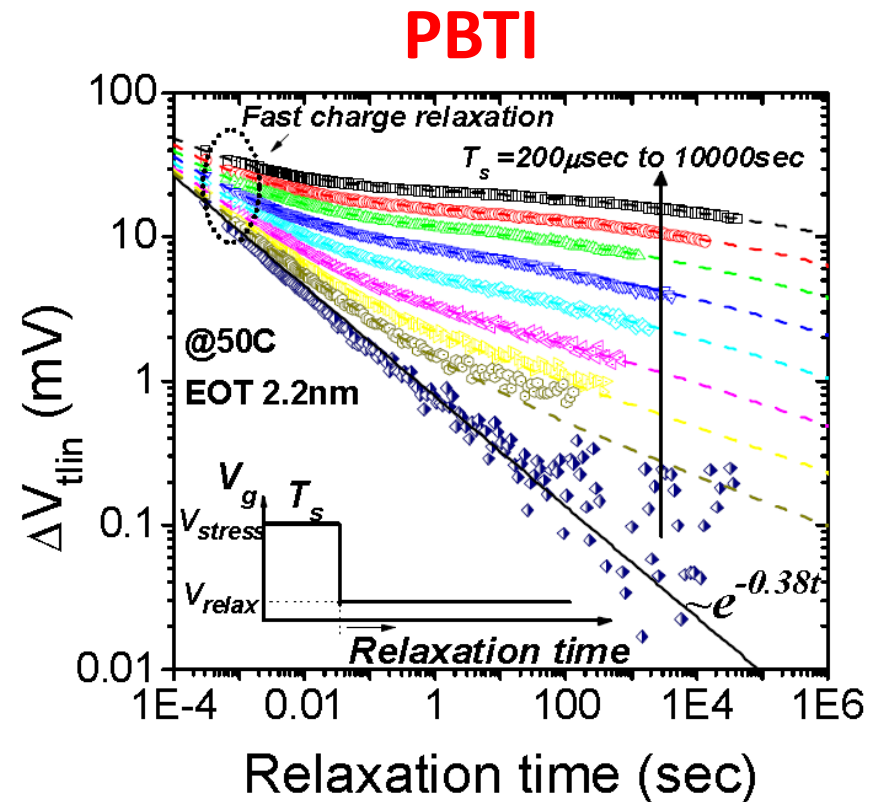
Design-in reliability → circuit solution to device reliability problem.

## Question:

What is the circuit impact of the fast transients in BTI?



Grasser, T. and B. Kaczer, ESSDERC 2007.



Zhao, K., J. Stathis, et al., IRPS 2012

# **Background**

**Standard BTI (n or p) reliability focus on “permanent” (non-recoverable) part of the degradation.**

**Most circuit reliability simulator follow this “simple” approach.**

**Some newer reliability simulator include the fast recovery, but mostly as degradation reduction.**

**A report has shown that the fast transient can cause SRAM failure**

**Another report showed that the fast transient can cause problem in analog circuit such as differential amplifiers and fast comparators.**

**The problem is largely considered a curiosity with little consequence.**

**The fast transients are the result of traps filling and emptying.**

As fabricated → some defects (hopefully low density).

After BTI stress → defect density increase.

Charges flow in during ON period →  $V_{TH}$  shift (reduce gate overdrive)

Charges flow out during OFF period →  $V_{TH}$  shift (recover gate overdrive)

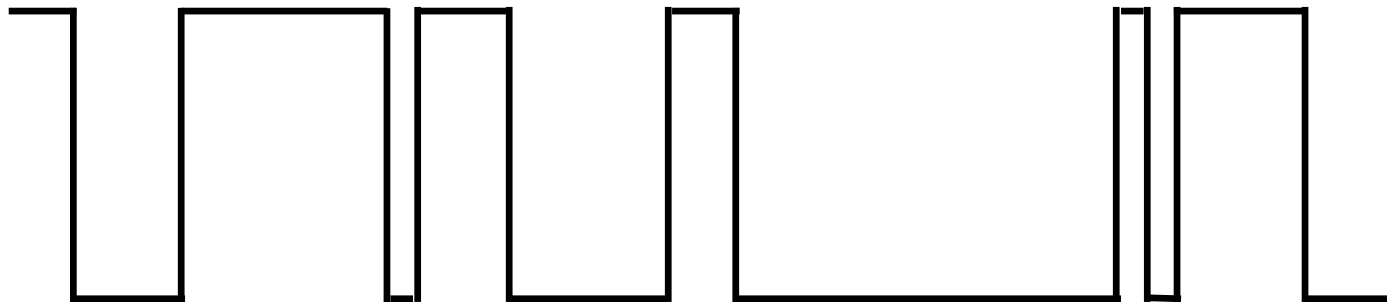
For a given defect density

Longer ON time → more complete trap filling

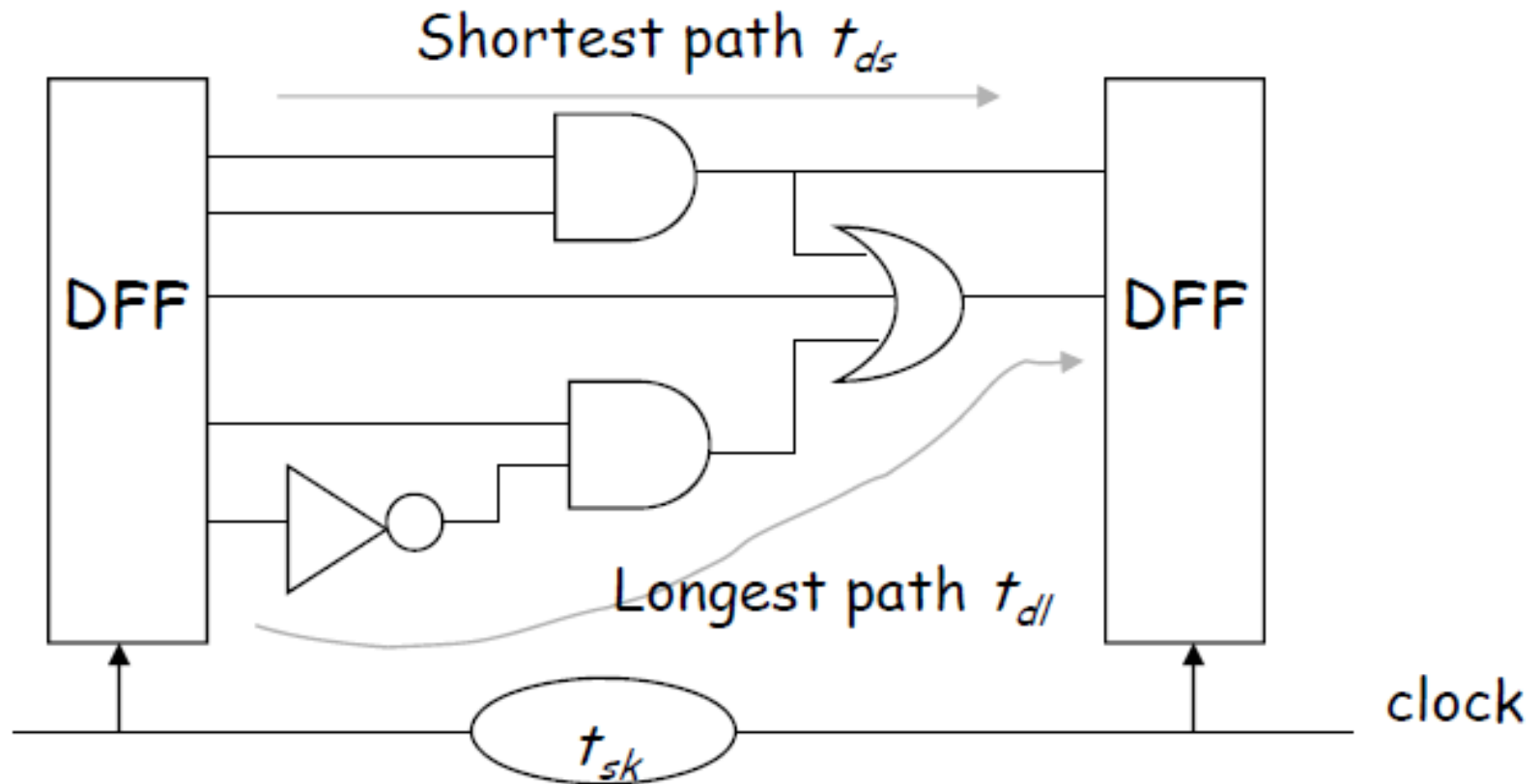
Longer OFF time → more complete trap emptying

**Effect is larger as the device ages.**

**For random logic running at high speed:**



**Significant increase in signal timing jitter (random skew) should be expected.**



To avoid setup time violation

$$+ \Delta t_{\text{degradation}} + \Delta t_{\text{randomskew}}$$

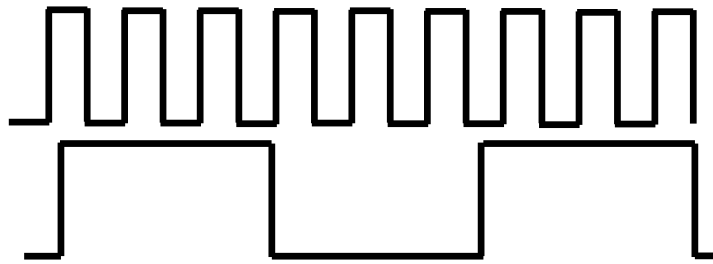
$$t_{\text{clk} \rightarrow Q} + t_{dl} + t_{\text{setup}} \leq T_{\text{clk}} + t_{sk}$$

To avoid hold time violation

$$+ \Delta t_{\text{degradation}} + \Delta t_{\text{randomskew}}$$

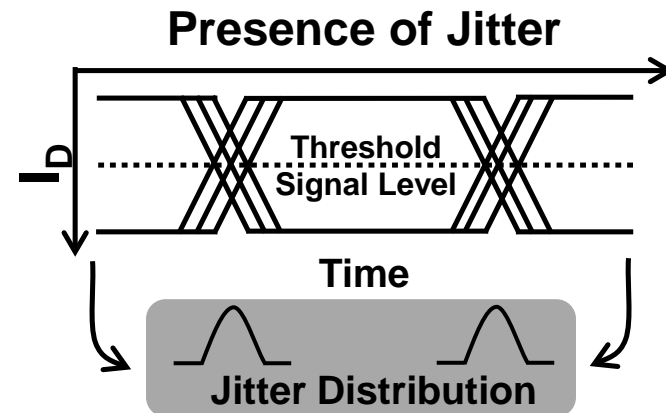
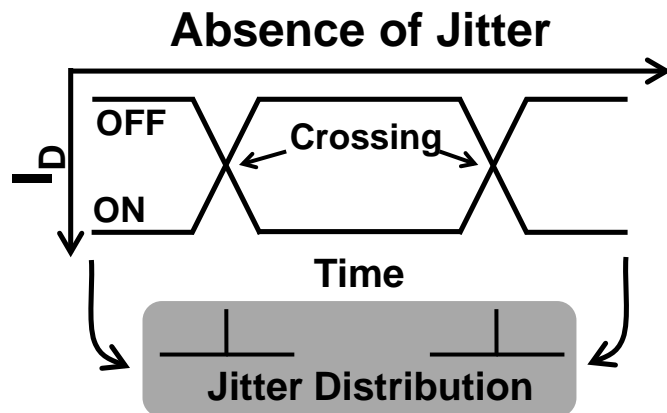
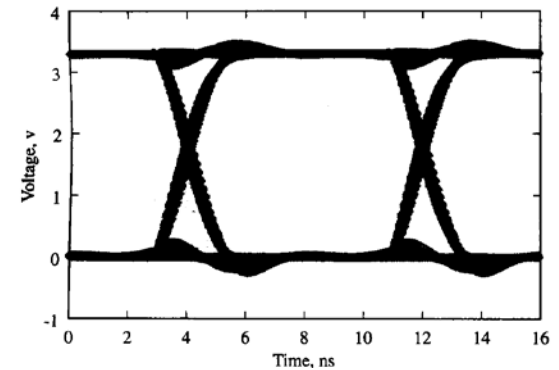
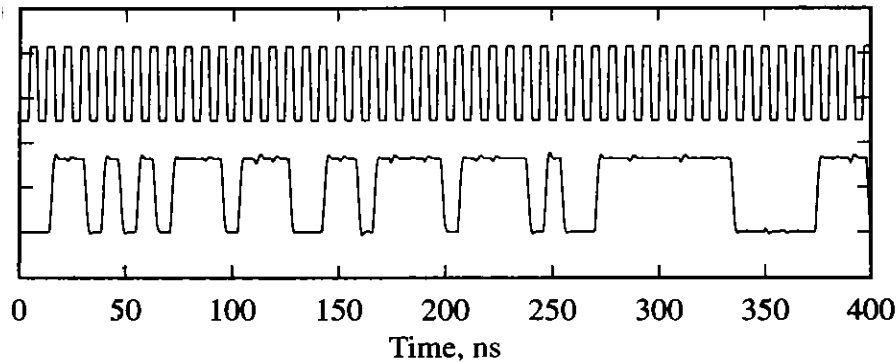
$$t_{\text{clk} \rightarrow Q} + t_{ds} \geq t_{\text{hold}} + t_{sk}$$

Ring oscillators cannot detect this effect ...

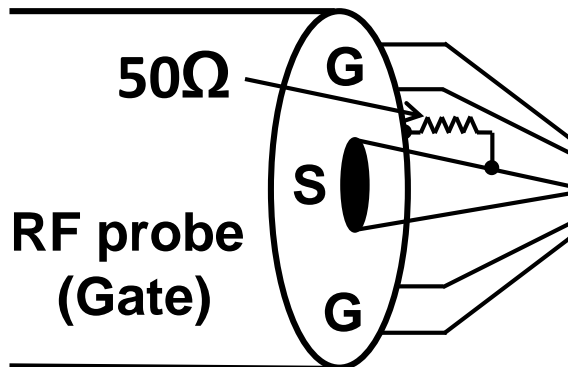
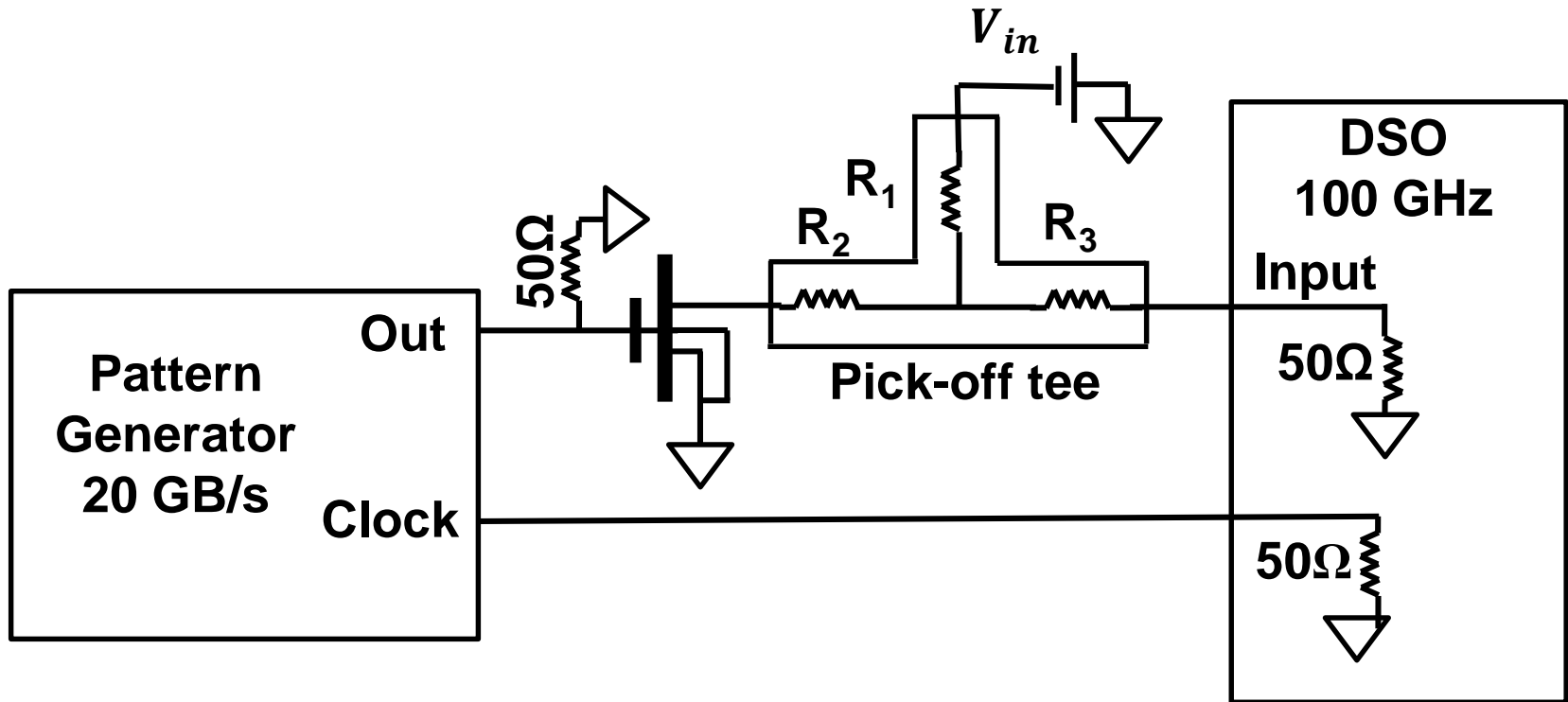


Constant ON and OFF time

For timing jitter in random bit pattern, eye diagram is a powerful technique.



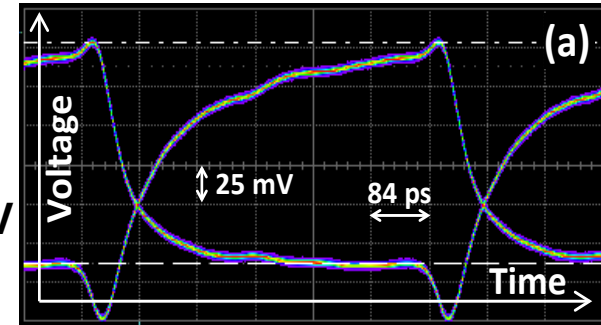
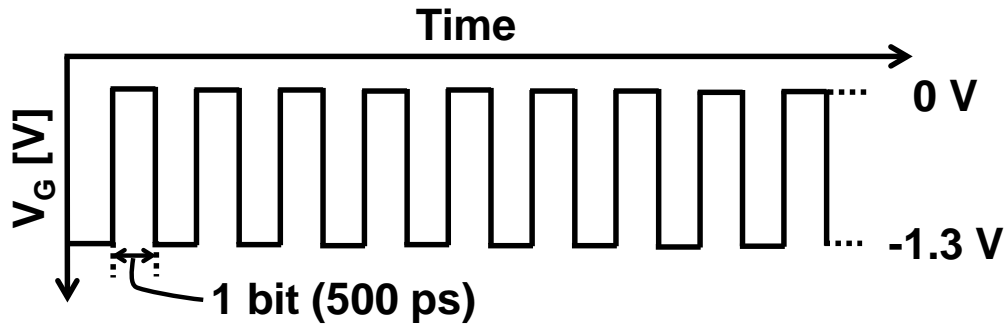
# Measurement Setup



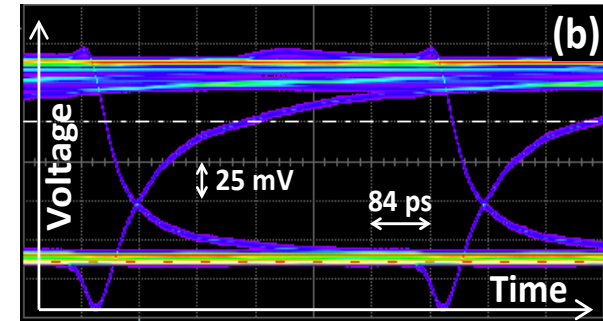
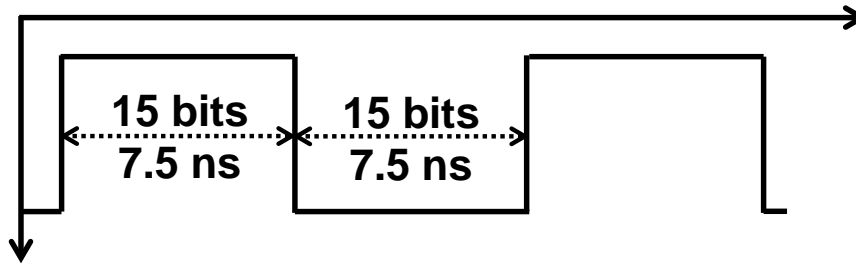
**Permits high-speed eye diagram and conventional “DC” measurements.**

# Gate Bit Patterns

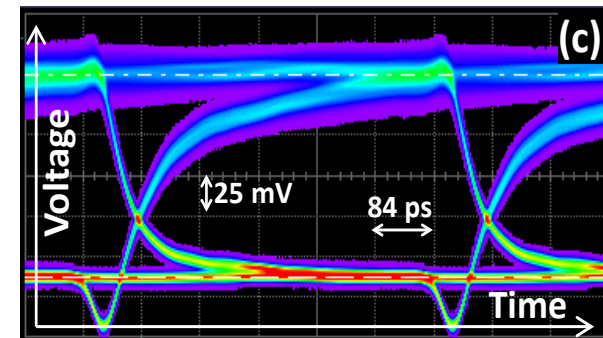
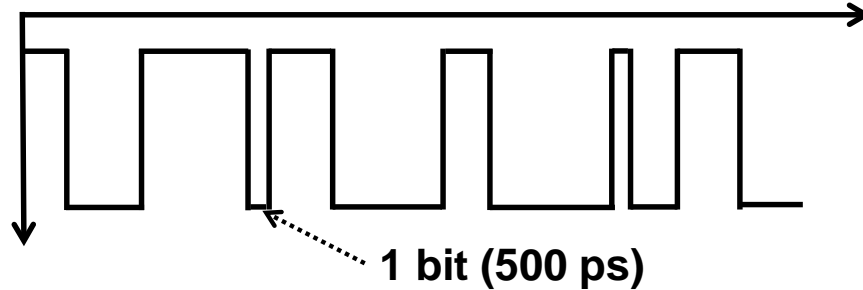
**Fast RO**  
32,000 bits



**Slow RO**  
30,000 bits



**PRBS15**  
32,767 bits



**Overshoot  $\rightarrow$  parasitic pad capacitance (480 fF).  
Limits bit rate to 2 Gbit/s.**

## Details

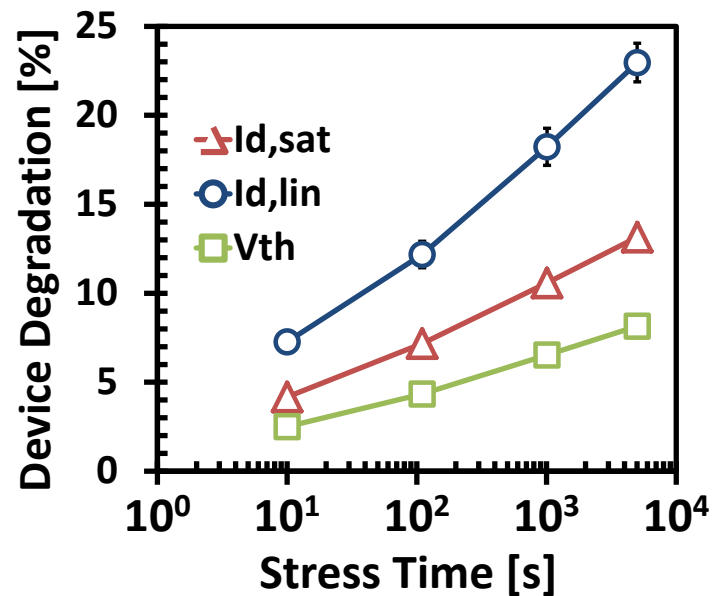
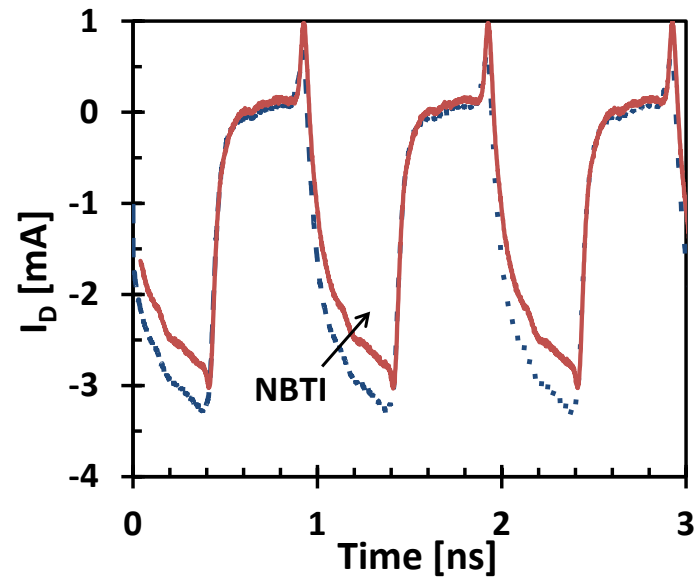
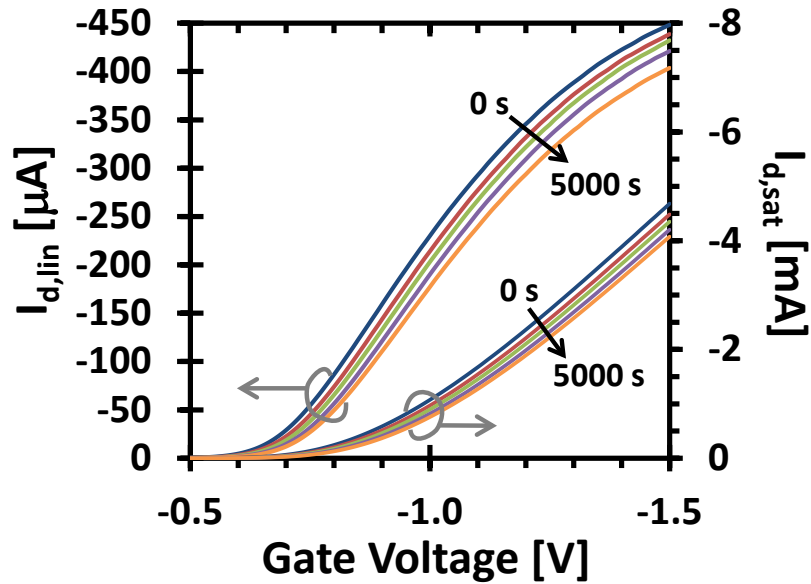
**10  $\mu\text{m}$  x 0.18  $\mu\text{m}$  GSG MOSFETs (1 nm  $\text{SiO}_2$ /2 nm  $\text{HfO}_2$ )**

**9 to 18 nominally identical devices for each condition**

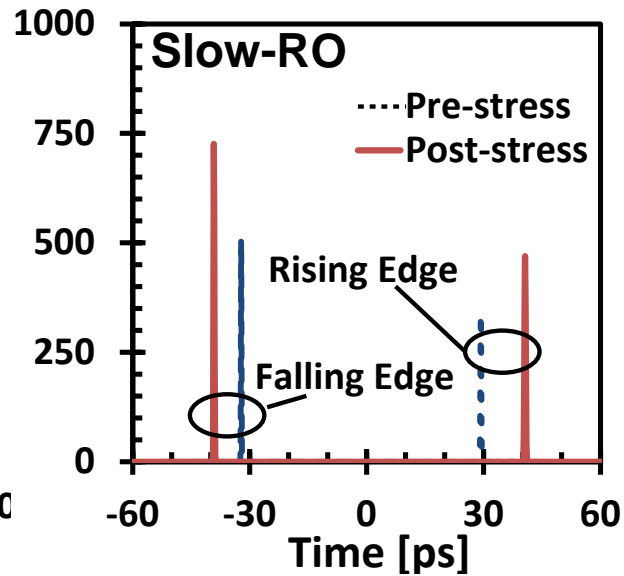
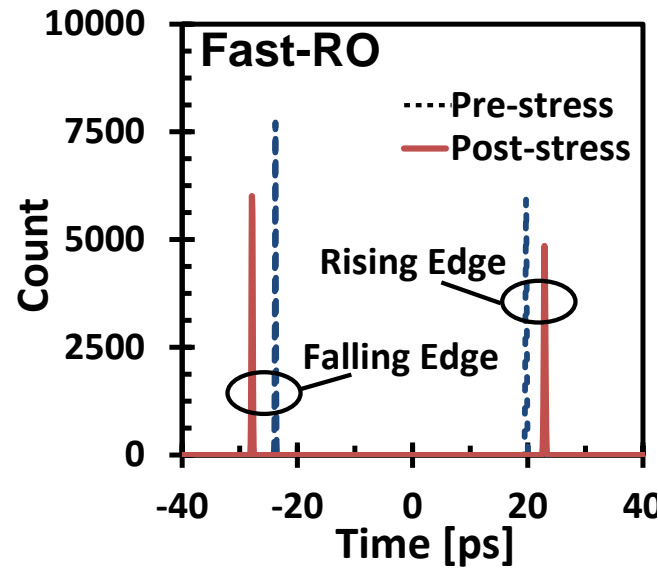
**Experimental sequence, all at 100 °C**

- **Measure**
  - Eye diagram at operation voltage.
  - DC parametric ( $V_{\text{th}}$ ,  $I_{\text{dlin}}$ , etc.).
- **Stress (various times) at acceleration voltage**  
+2V for PBTI and -2V for NBTI
- **Recovery**
  - All contacts floating for several hundred seconds.
- **Measure and repeat**

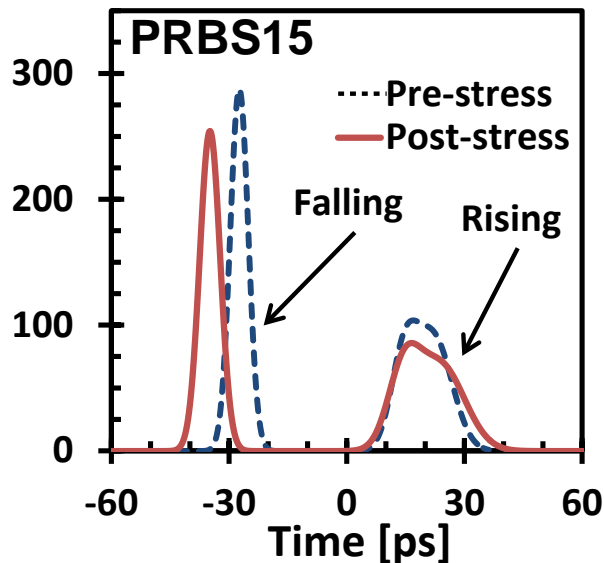
# NBTI Degradation



# NBTI continue ...

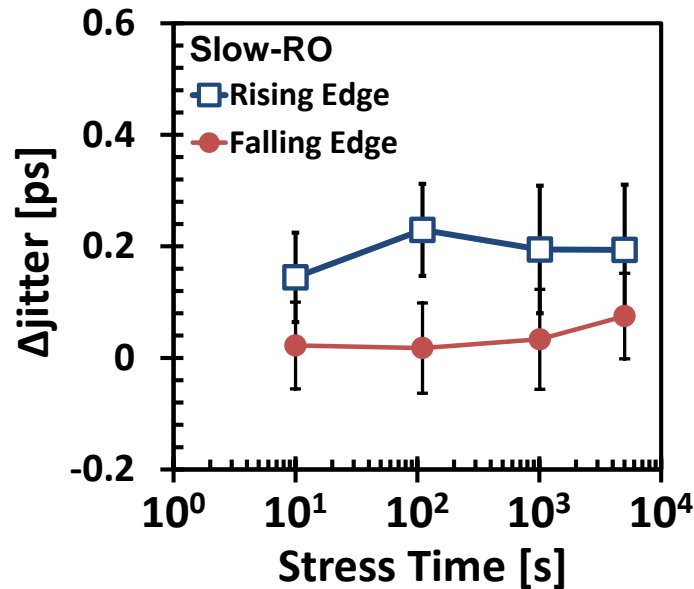
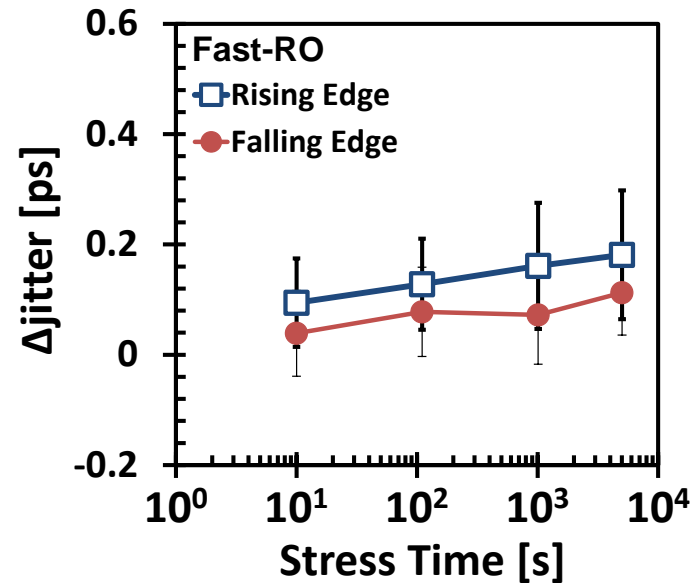


Large timing shifts  $\propto$  to  $V_{th}$ .  
---- Expected and captured in RO studies

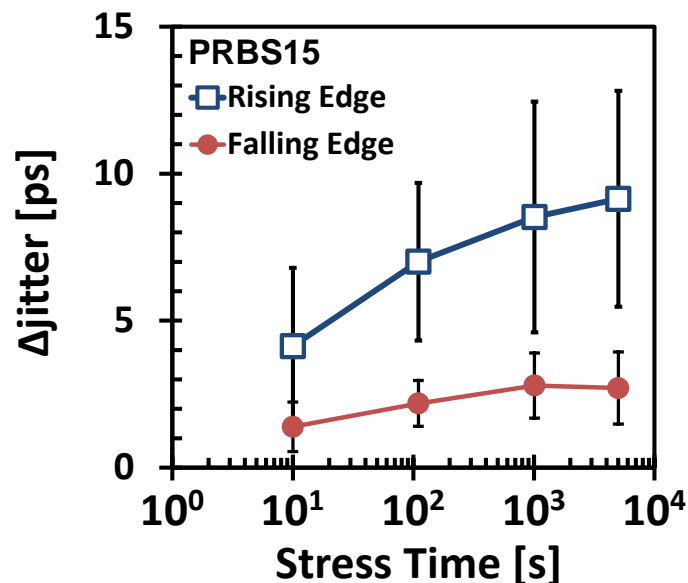


**PRBS15 – peak width increase.**  
**Random timing jitter.**  
**Not observable in RO studies.**

# As a function of stress time ...



Jitter increase  
negligible for RO



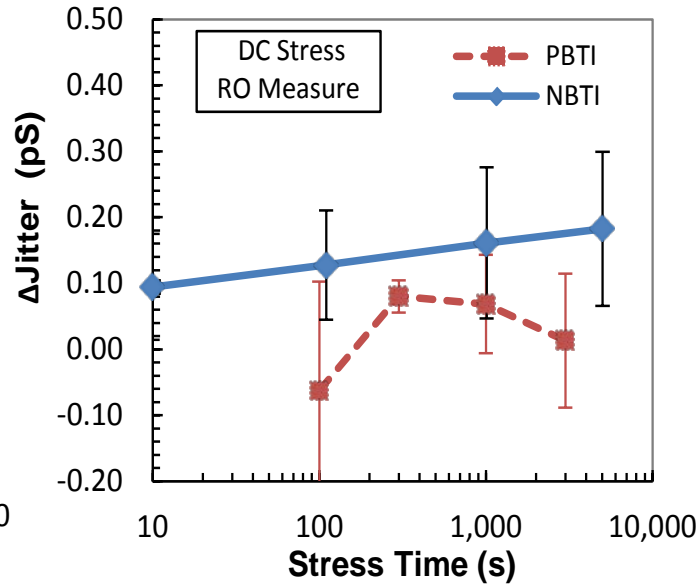
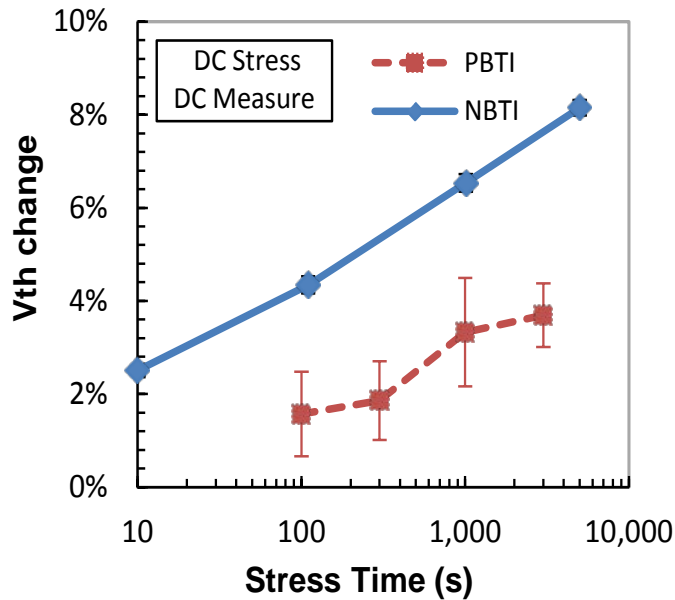
**Large jitter increase for PRBS15.**

— Consistent with stress induced  $V_{th}$  increase (defect generation).

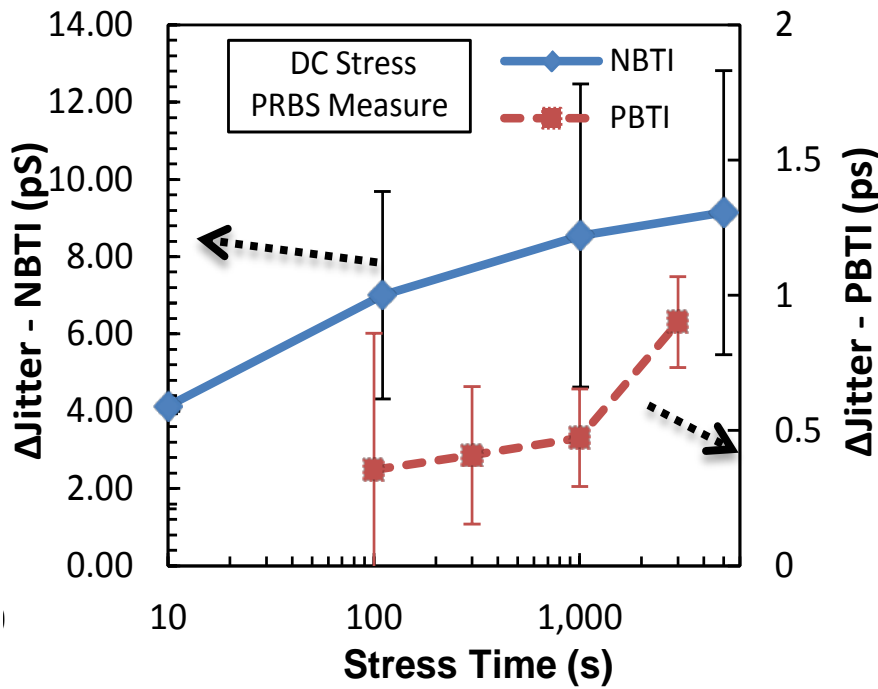
Recall: measure is after long (600s) relaxation.

**Note that this is from one transistor!!!**

# For PBTI ...



Similar to NBTI case, no meaningful jitter increase in RO.

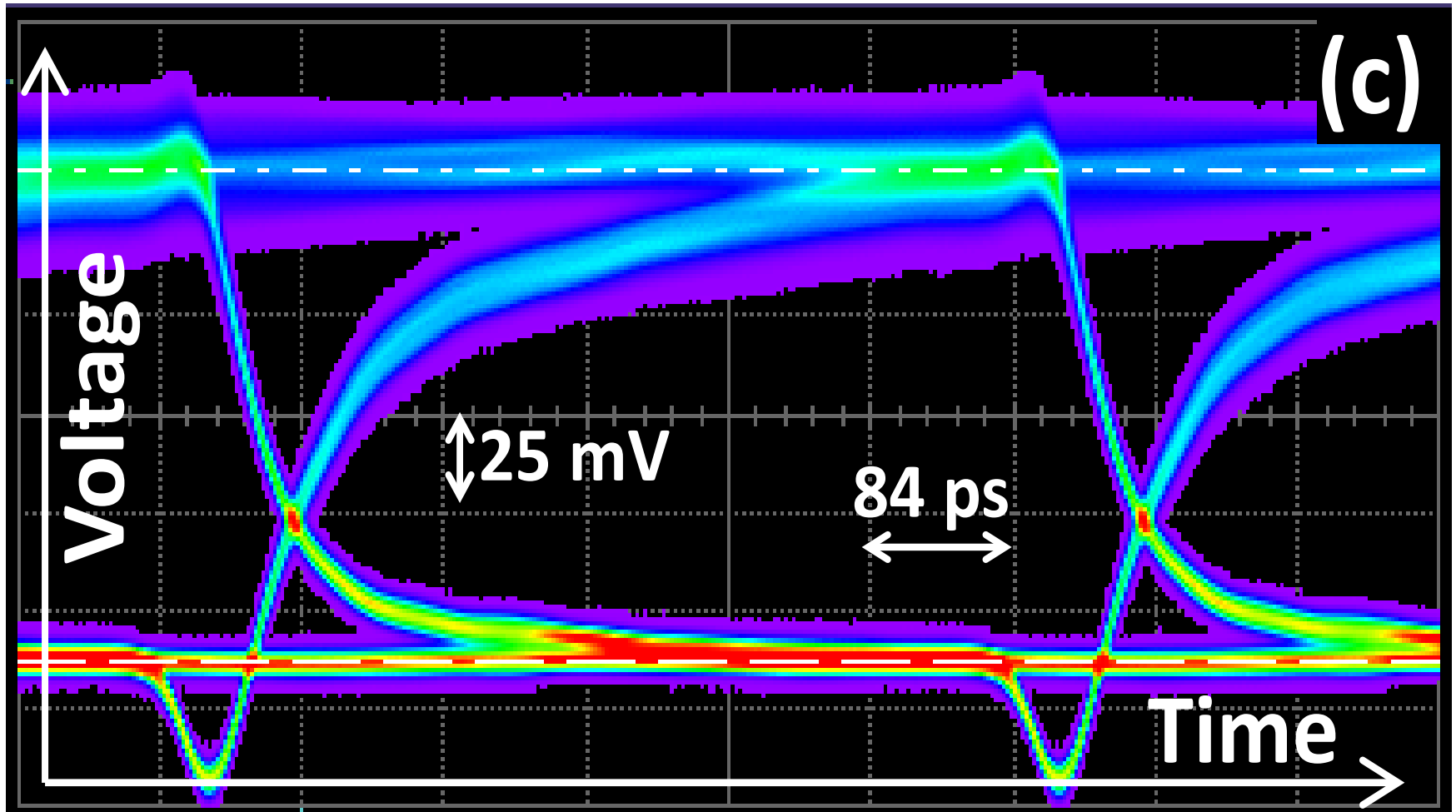


PBTI degradation is ~40% of NBTI for similar stress level.

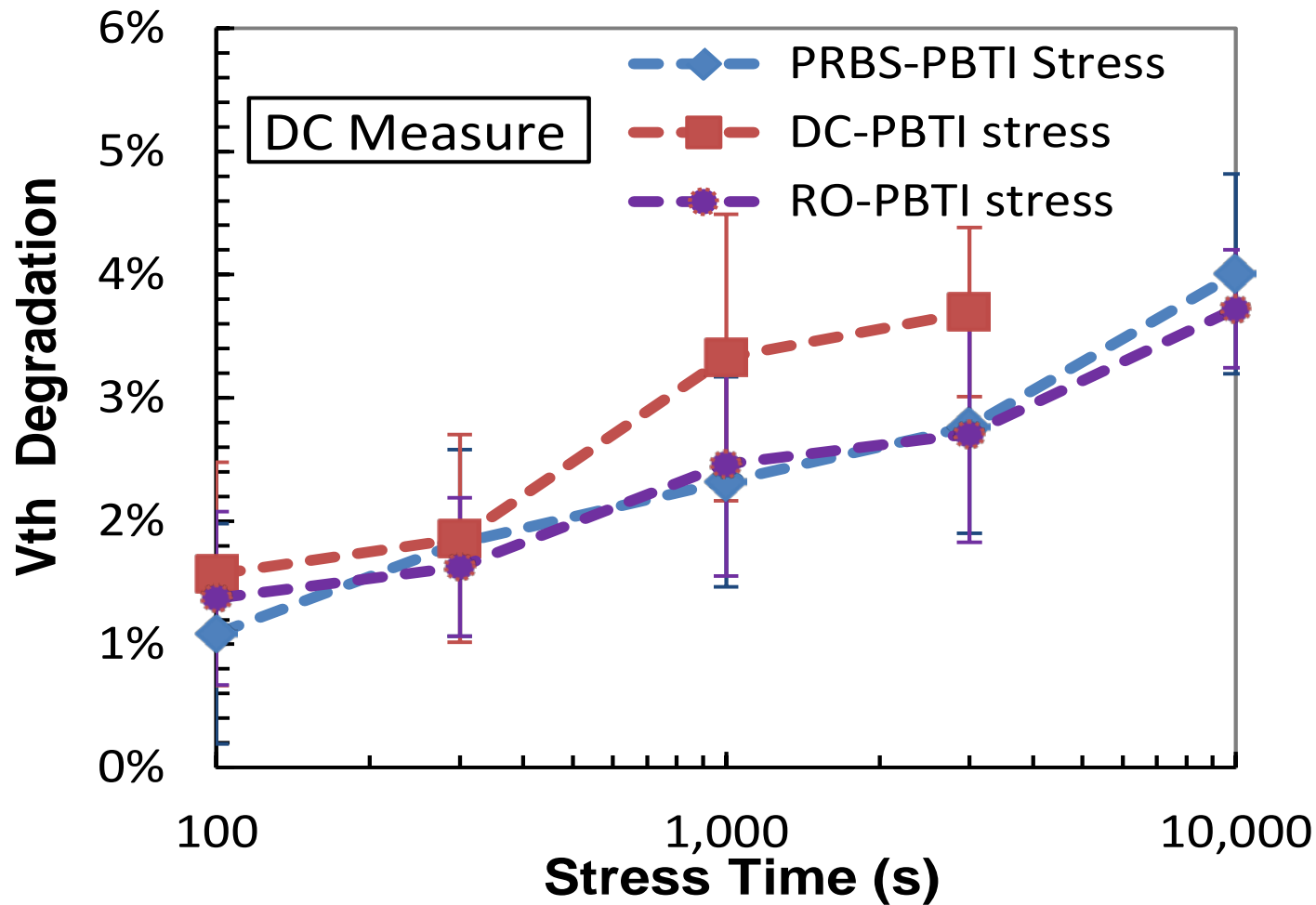
Jitter increase is ~10% of NBTI for similar stress level.

The small jitter increase may or may not be due to random trap filling and emptying...

A part of the jitter increase is simply the result of lower ON current



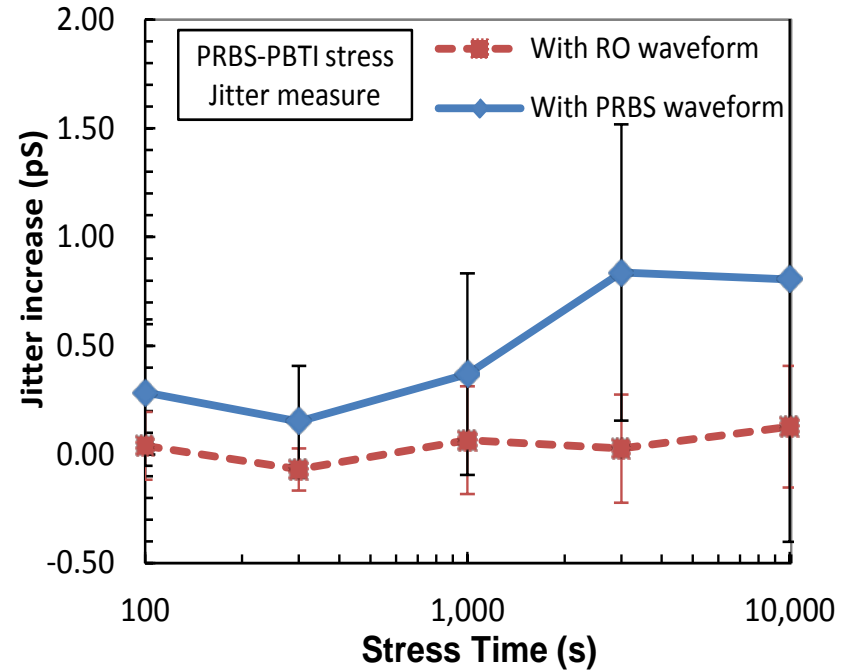
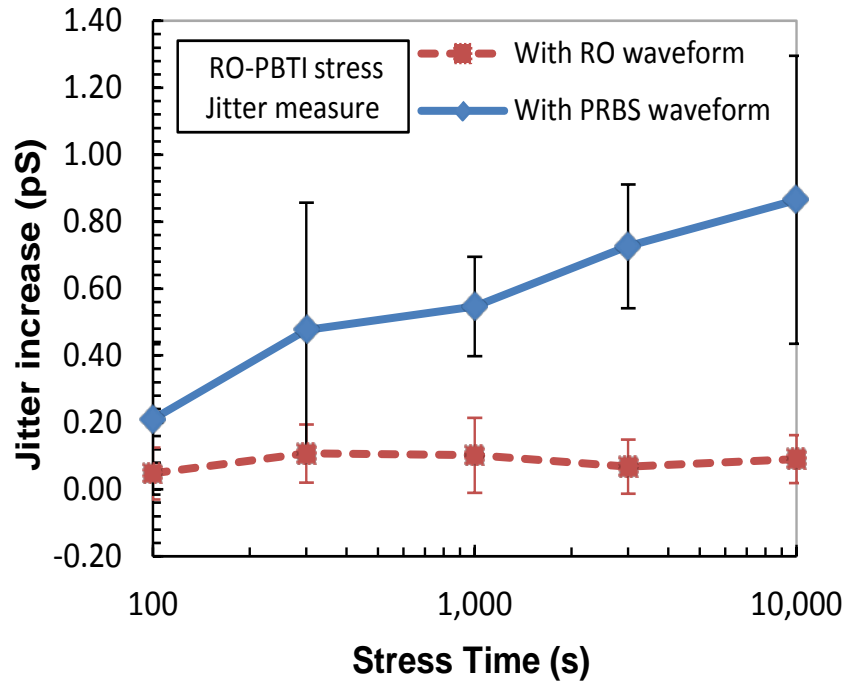
**Random bit pattern can also be used for stress to mimic real circuit ...**



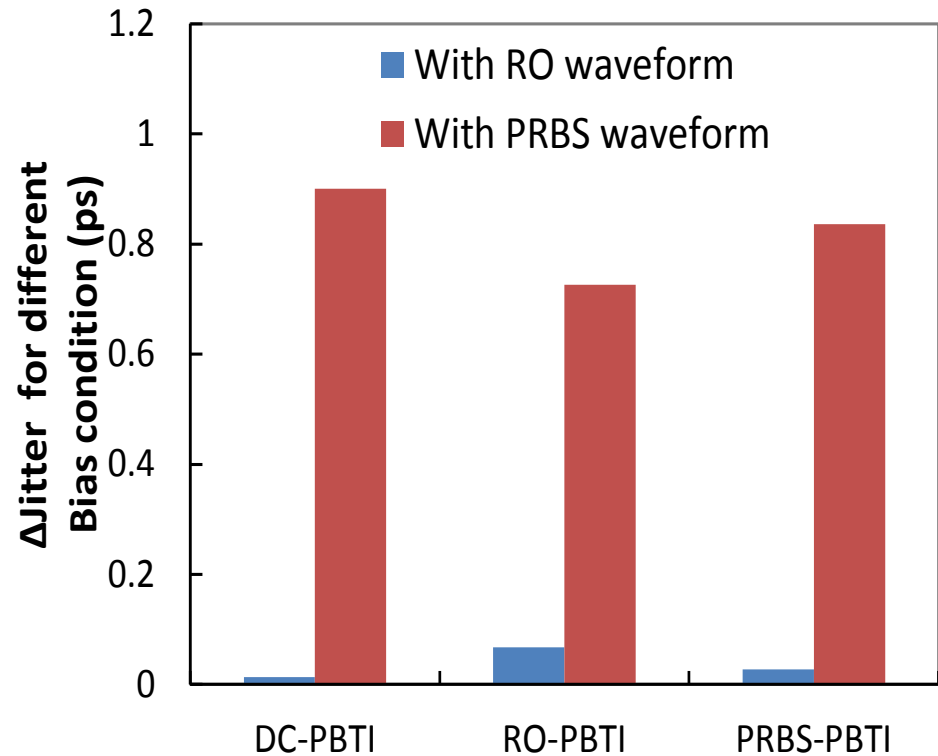
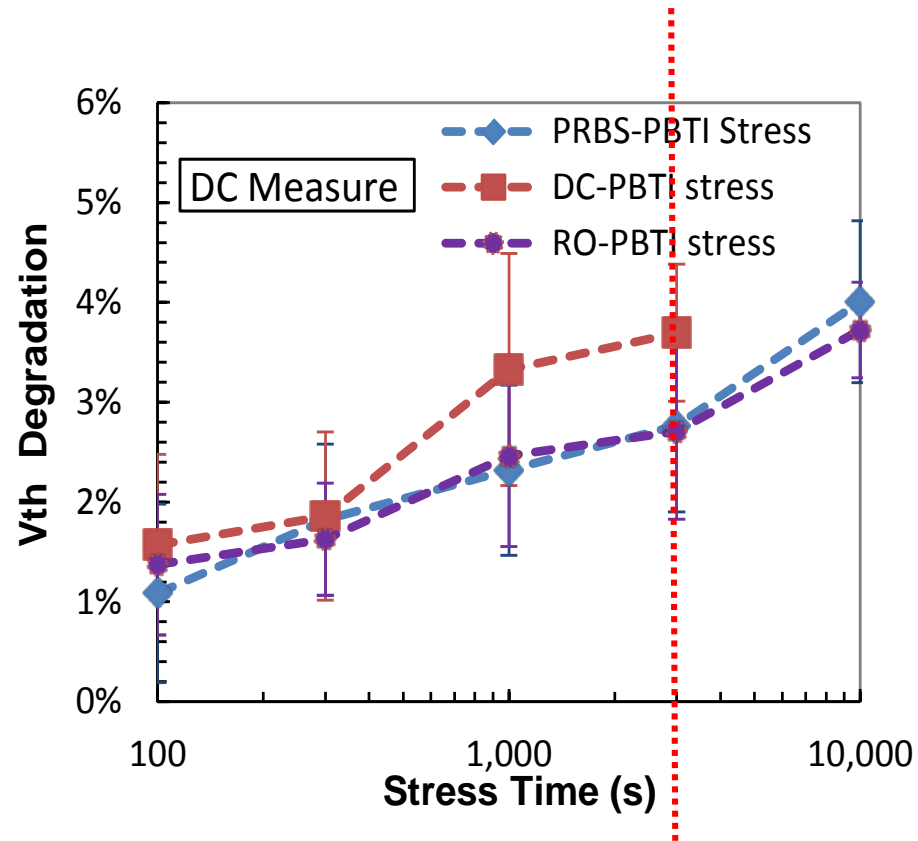
**For PBTI, random bit pattern stress is similar to AC stress – 50% average duty cycle.**

**No frequency effect ...**

## Jitter increase is also similar



**Surprise: under same stress, DC stress produces more degradation, but the jitter increase is similar for all three stress types.**



**From jitter perspective, AC stress does not have more margin than DC stress.**

# **Summary**

**Transients due to charge flowing in and out of traps can produce large random  $V_{TH}$  fluctuation under random logic operation, leading to significant timing jitter (random skew).**

**Eye diagram is a very suitable method to investigate this problem.**

**The timing jitter increase is very large (in case you forget, the data are from a single transistor) when consider large logic depth.**

**For PBTI, the jitter increase is much smaller than NBTI.**

**For PBTI, random bit pattern stress is similar to AC stress, suggesting pure duty factor effect and no frequency dependent.**

**For PBTI and from jitter perspective, DC and AC stress produce similar degradation.**